Advanced packaging and heterogeneous integration

Optical metrology solutions for next-generation semiconductors

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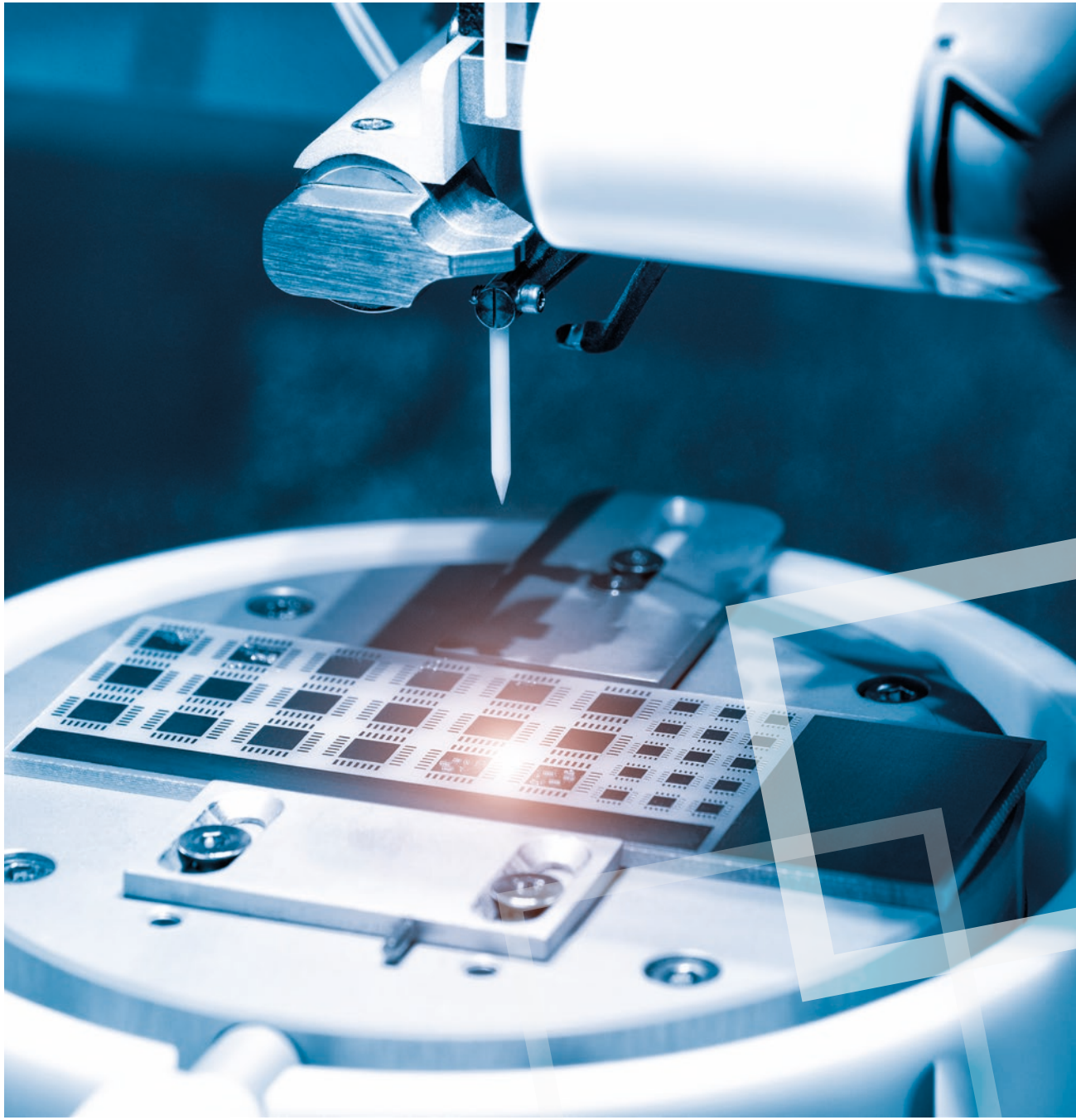
ADVANCED PACKAGING

Advanced packaging techniques vary in complexity and design, each offering unique advantages for improving performance, integration density, and energy efficiency.

2.5D integration enhances connectivity by placing multiple dies side by side on a silicon or organic interposer, which serves as a high-density routing layer. This approach reduces power consumption and increases bandwidth, making it ideal for High Bandwidth Memory (HBM) integration with GPUs and AI accelerators. One of the most famous 2.5D integrations is Chip-on-Wafer-on-Substrate (CoWoS®).

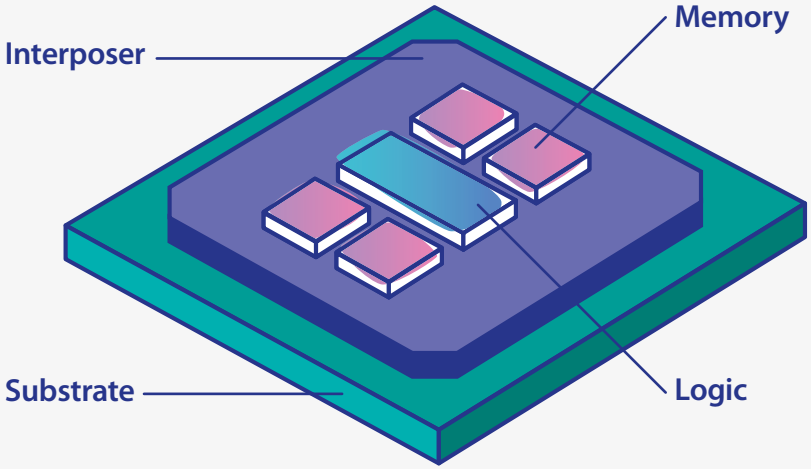
For even greater integration, 3D packaging vertically stacks multiple dies, interconnecting them through Through-Silicon Vias (TSV)—microscopic vertical channels that allow direct electrical communication between layers. This architecture significantly reduces data transfer distances, improving speed and efficiency while minimizing power loss. 3D integration is widely adopted in high-density memory solutions like 3D NAND flash and advanced processor architectures like Intel's Foveros technology.

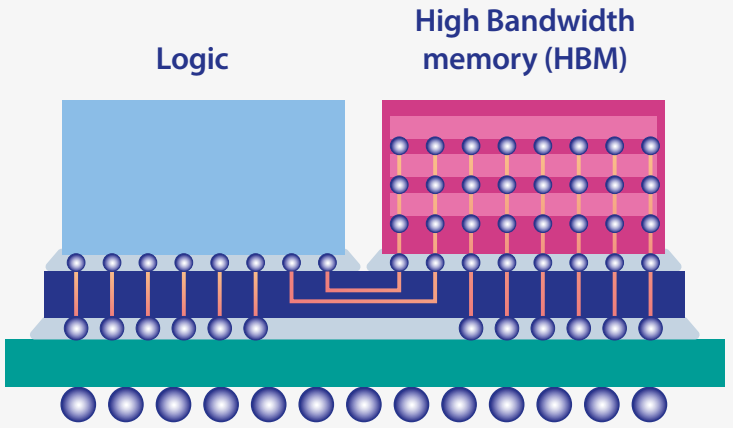


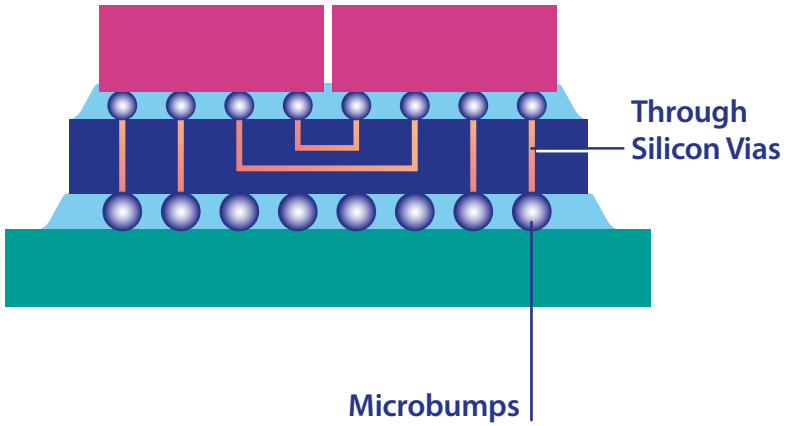
Micro bumps and hybrid bonding are crucial enablers of both 2.5D and 3D integration, two ways to create very high-density wafer-to-wafer or die-to-wafer interconnects.

Beyond 2.5D and 3D integration, wafer-level and panel-level packaging have emerged as key strategies for improving efficiency, yield, and scalability in advanced semiconductor manufacturing. Wafer-level packaging (WLP) processes entire wafers before singulation, enabling finer interconnect pitches and reducing package size. Fan-Out Wafer-Level Packaging (FOWLP) enhances this by expanding interconnects beyond the die footprint, improving thermal management and I/O density, making it ideal for mobile and high-performance applications. Fan-Out Panel-Level Packaging (FOPLP) further increases production efficiency by processing chips on larger rectangular panels, lowering costs and material waste, particularly in high-volume applications like automotive electronics.

These advanced packaging methods introduce significant metrology challenges, requiring precise measurements of TSV depths, microbump heights, interconnect alignment, and bonding surface roughness. High-resolution 3D optical metrology plays a critical role in ensuring process accuracy, optimizing performance, and minimizing defects in next-generation semiconductor packaging.

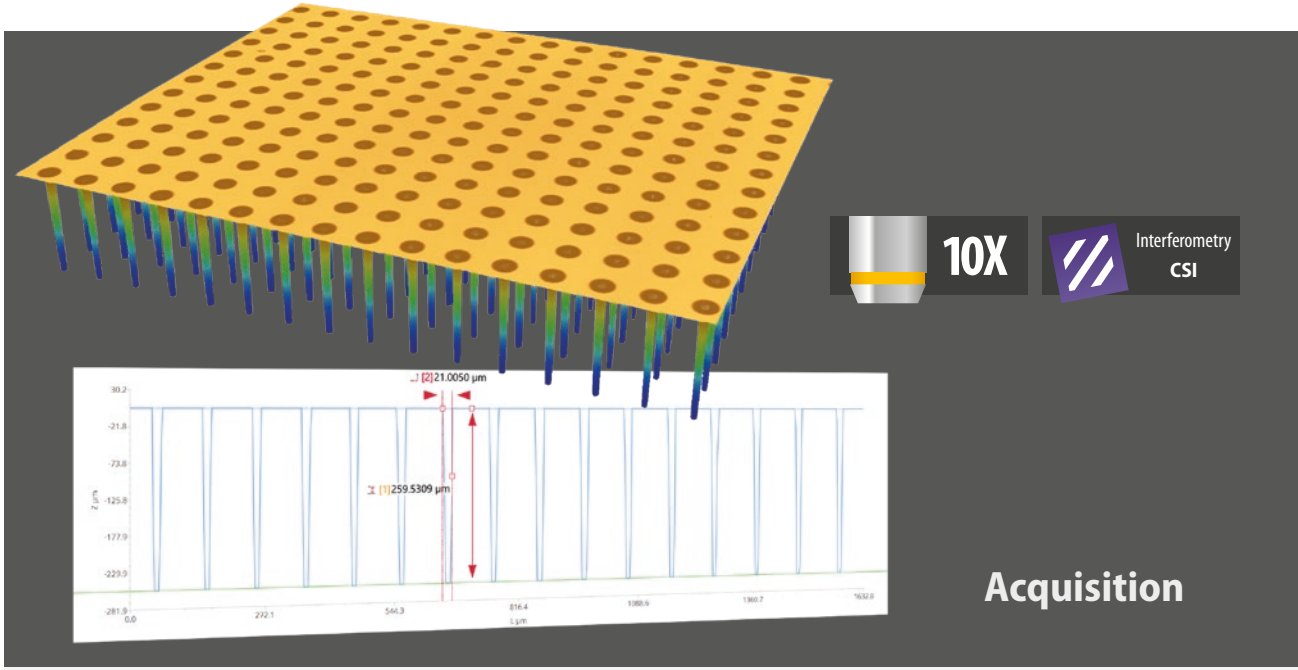




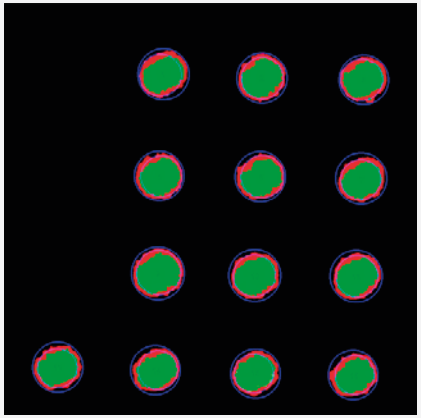


THROUGH SILICON VIAS

One key parameter to characterize these advanced semiconductor architectures is the depth of the interposer layer. This layer is designed to be as thin as possible to minimize the space it occupies. The challenge lies in accurately measuring through these small but deep holes, which can be measured using the S neox and Interferometry with low magnification.

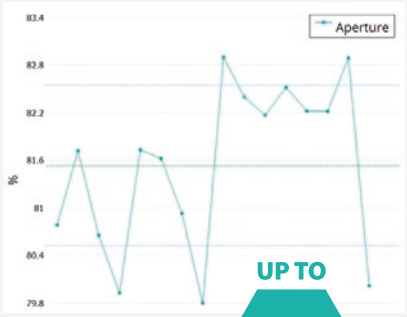


Analysis



Hole

SensoPRO Plugins



Depth	55.5053	µm
TopDiameter	67.1318	µm
BottomDiameter	55.6473	µm
Space	77.9965	µm
SpaceAvg	95.8276	µm
Aperture	82.8926	%
MIC	60.7793	µm
MCC	73.6116	µm
Roundness	82.5676	%
TopSa	0.3451	µm
BottomSa	4.9104	µm
BottomSp	2.6141	µm
BottomSv	3.7889	µm
MaxDepth	58.1194	µm
MinDepth	59.2942	µm
DepthRange	1.1748	µm
Pit	2.6141	µm
DP-TD	0.8268	

UP TO **17** PARAMETERS

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